AMENDMENTS TO THE CLAIMS:

Please cancel claim 24 without prejudice or disclaimer.

1. (Currently amended) A method of analyzing voltage drops on at least one power grid in an integrated circuit chip, comprising:

dividing a clock period ~~cycle~~ of said integrated circuit chip into a plurality of time periods;

performing a static timing analysis to obtain current waveform data for said plurality of time periods for a plurality of cells within said at least one power grid of said integrated circuit chip; and

performing at least one simulation of said at least one power grid using extracted power grid information within said at least one power grid, placement information for said plurality of cells, and said current waveform data to calculate at least one voltage at a plurality of locations within said power grid.

2. (Previously presented) The method according to claim 1, wherein said performing said static timing analysis comprises using pre-characterized cell library information.

3. (Previously presented) The method according to claim 1, further comprising:
computing at least one current density on at least one element of said power grid.

4. (Previously presented) The method according to claim 3, further comprising:
modifying said integrated circuit chip based on said at least one current density.

5. (Canceled)

6. (Previously presented) The method according to claim 1, further comprising:

modifying said integrated circuit chip based on said at least one voltage.

7-9. (Canceled)

10. (Previously presented) The method according to claim 1, wherein each of said time periods is greater than or equal to at least one of rise and fall times of a predetermined fraction of signals on said integrated circuit chip.

11. (Previously presented) The method according to claim 1, wherein said at least one voltage comprises a voltage during each of said plurality of time periods.

12. (Previously presented) The method according to claim 3, further comprising:

checking said voltages against allowable limits; and

checking said at least one current density against at least one of electromigration limits and local heating rules.

13. (Previously presented) The method according to claim 1, further comprising:

performing another static timing analysis using said at least one voltage determined in said performing said at least one simulation of said at least one power grid.

14. (Previously presented) The method according to claim 1, further comprising:

generating a graphical map of said at least one voltage and said plurality of locations.

15. (Currently amended) A system for analyzing power distribution in an integrated circuit chip comprising:

a chip design device which uses ~~for using~~ pre-characterized cell data to logically and physically design said integrated circuit chip;

a power grid extracting device which inputs ~~, for inputting~~ physical design data from said

chip design device and generates ~~generating~~ extracted signal net information; and

a static timing analysis tool which divides ~~, for dividing~~ a clock period ~~cycle~~ of said integrated circuit chip into a plurality of time periods, and inputs ~~inputting~~ said extracted signal net information and said physical design data and generates ~~generating~~ current waveform data for said time periods.

16. (Currently amended) The system according to claim 15, further comprising:

a power distribution analysis tool which reads as input ~~, for inputting~~ said current waveform data and ~~generating~~ power distribution data and creates node voltage information.

17. (Previously presented) The method according to claim 6, wherein said method is performed by using a digital data processing apparatus.

18. (Currently amended) A programmable storage medium tangibly embodying a program of machine-readable instructions executable by a digital processing apparatus to perform a method of analyzing voltage drops on at least one power grid in an integrated circuit chip, said method comprising:

dividing a clock period ~~cycle~~ of said integrated circuit chip into a plurality of time periods;

performing a static timing analysis to obtain current waveform data for said plurality of time periods for a plurality of cells within said at least one power grid of said integrated circuit chip; and

performing at least one simulation of said at least one power grid using extracted power grid information, placement information for said plurality of cells, and said current waveform data to calculate at least one voltage at a plurality of locations within said power grid.

19. (Previously presented) The system according to claim 15, wherein said pre-characterized cell data is included within a pre-characterized cell library.

20. (Original) The system according to claim 15, wherein said pre-characterized cell data comprises charge data, timing data, voltage data, temperature data, load data, input slew rate data, direct current data and process corner data.

21. (Currently amended) The system according to claim 15, wherein said power grid extracting device extracts parasitic resistors, capacitors and inductors from a physical design of said integrated circuit chip ~~to generate extracted signal net information~~.

22. (Original) The system according to claim 15, wherein said current waveform data generated during an operation of said system is input to said chip design device during a next operation of said system to refine a physical design of said integrated circuit chip.

23. (Currently amended) The system according to claim 15, wherein said static timing analysis tool determines when a current is required on said integrated circuit chip, and an amount of current required on said integrated circuit chip~~, and where current is required on said integrated circuit chip~~.

24. (Canceled)

25. (Original) The system according to claim 15, wherein said static timing analysis tool disregards circuits which cannot switch during a same time period.

26. (Currently amended) The system according to claim 15, wherein each of said time periods is greater than or equal to a rise or fall time that captures a predetermined fraction ~~95%~~ of signals on said integrated circuit chip.

27. (Currently amended) The system according to claim 15, wherein said static timing

analysis tool assigns a charge used by a circuit to at least one time period~~, and calculates node voltages for each time period~~.

28. (Currently amended) The system according to claim 27, wherein said power distribution ~~static timing~~ analysis tool checks calculated node voltages against allowable limits, electromigration rules and local heating rules, and calculates current densities using said calculated node voltages.

29. (Currently amended) The system according to claim 28, wherein node voltages calculated during a static timing analysis are back annotated into said power distribution ~~static timing~~ analysis tool during a next static timing analysis to re-calculate node voltages.

30. (Original) The system according to claim 16, wherein said power distribution analysis tool generates a graphical map of a power distribution on said integrated circuit chip.

31. (Previously presented) The programmable storage medium according to claim 18, wherein said performing said static timing analysis comprises using pre-characterized cell library information.

32. (Previously presented) The programmable storage medium according to claim 31, wherein said method further comprises:

computing at least one current density on at least one element of said power grid.

33. (Previously presented) The programmable storage medium according to claim 31, wherein said method further comprises:

modifying said integrated circuit chip based on said at least one current density.

34. (Canceled)

35. (Previously presented) The programmable storage medium according to claim 18, wherein said method further comprises:

modifying said integrated circuit chip based on said at least one voltage.

36. (Original) The programmable storage medium according to claim 18, wherein said static timing analysis comprises:

disregarding circuits which cannot switch during a same time period.

37. (Previously presented) The programmable storage medium according to claim 18, wherein said at least one voltage comprises a voltage during each or said plurality of time periods.

38. (Previously presented) The programmable storage medium according to claim 32, wherein said method further comprises:

checking said voltages against allowable limits; and

checking said at least one current density against at least one of electromigration limits and local heating rules.

39. (Previously presented) The programmable storage medium according to claim 38, performing another static timing analysis using said at least one voltage determined in said performing said at least one simulation of said at least one power grid.

40. (Previously presented) The programmable storage medium according to claim 18, wherein said method further comprises:

generating a graphical map of said at least one voltage and said plurality of locations.